CERTIFICATION OF TRANSLATION

I, Hiroshi Takayama, residing at 6th Floor, Shin-Yokohama IC Building, 18-9, Shin-Yokohama 3-chome, Kohoku-ku, Yokohama-shi, Kanagawa Japan, state:

that I know well both the Japanese and English languages;

that I translated, from Japanese into English, the specification and claims as filed in U.S. Patent Application No. 60/420,788, filed October 24, 2002; and

that the attached English translation is a true and accurate translation to the best of my knowledge and belief.

December 12, 2003
Date

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Specification

[Title of the Invention]

Method of Processing Process Subject

[Field of the Invention]

The present invention relates to a process performed in the process of manufacturing semiconductor devices, and particularly to a process of improving the plasma resistance of a mask layer, and a process of plasma etching and a process of removing a mask layer with plasma (ashing), both of which are performed thereafter.

[Conventional Art]

When plasma etching is performed on an etching objective layer, a resist mask formed of, e.g., a photoresist is used. Particularly, in accordance with demands for micro-patterning, a photoresist frequently used in recent years is an ArF photoresist, i.e., a photoresist to be exposed to laser light from a light source of ArF gas, which is suitable for forming an opening pattern of about 0.13 m or less.

However, since the ArF photoresist layer has a low plasma resistance, it causes a problem in that the surface of the photoresist layer becomes rough during etching. If the surface of the photoresist layer

becomes rough, the shapes of opening portions are deformed with the etching progress, thereby making it difficult to obtain the designed shapes of etched holes or etched grooves. Furthermore, during etching, the photoresist disappears at some positions, and the etching proceeds to portions that are designed to be non-etched.

As a method of improving the plasma resistance of a photoresist layer, there is a method of irradiating the surface of a photoresist layer with ultraviolet rays, an electron beam, or an ion beam, a method of heat-setting a photoresist, or a method of applying heat or light energy to an organic silicon compound to coat the surface of a photoresist layer with a thin cured layer.

In the above-described methods of improving the plasma resistance of a photoresist layer, it is necessary to perform a process of improving the plasma resistance in a container other than a container used in an etching step performed thereafter. Since a process subject to be processed needs to be transferred from the container for performing the process of improving the plasma resistance of a photoresist layer to the etching container, the yield is lowered in the transfer step and throughput is lowered due to a necessary transfer time. Furthermore, since the container for performing the process of improving the

plasma resistance needs to be provided independently of the etching container, not only an additional space is required, but also the cost increases.

The etching container may be provided additionally with ultraviolet ray radiating means or heating means without independently disposing a container for performing the process of improving the plasma resistance. In this case, however, since the structure still requires the ultraviolet ray radiating means or heating means, the cost also increases.

[Disclosure of Invention]

In order to solve the problems described above, a first invention is directed to the point that sputtering is performed to form a silicon-containing layer on the surface of a mask layer that covers an etching objective layer and has an opening formed therein. The silicon-containing layer formed on the surface of the mask layer improves the plasma resistance of the mask layer. Particularly, where the mask layer is made of an ArF photoresist layer, which has a relatively low plasma resistance, the plasma resistance is remarkably improved. Although the ArF photoresist is described as an example of a mask having a low plasma resistance, the present invention may be applied to another mask having a low plasma resistance. The sputtering can be performed in a process container

to be used in a plasma etching step performed thereafter, this is advantageous as compared to a conventional method of improving the plasma resistance which requires an additional device, such as heating means or a light source.

A sputtering target used at this time is a member having a surface at least a part of which is made of silicon, disposed in the process container. Specifically, it may be a focus ring disposed around the process subject, a showerhead disposed to supply an etching gas into the process container, or a silicon member put in as a target. Where the process container is of the type that processes a plurality of semiconductor wafers, a wafer having undergone no device processes (bare wafer) may be used as a target. Even where the process container is of the type that processes a single semiconductor wafer, a silicon-exposed portion prepared outside a device region may be used as a target. Furthermore, if a semiconductor wafer is designed in advance to have a silicon-exposed portion within a device region, the exposed portion may be used as a target. The silicon used in the sputtering consists preferably of single-crystal.

The sputtering is performed as follows, for example. Specifically, a process container is prepared such that a member having a surface at least a part of which is made of silicon and a process subject are

present in the process container. In this state, an inert gas, such as Ar, Kr, or Xe, is supplied into the process container, and energy is applied to ionize at least a part of the inert gas. High-frequency energy, microwave energy, or the like may be used as the energy. The high-frequency energy may be supplied by applying a high-frequency power to an antenna, or by applying a high-frequency power to a plate electrode. The ionized inert gas acts on the member having a surface at least a part of which is made of silicon, to discharge silicon-containing substances therefrom. The discharged silicon-containing substances stick mainly to the surface of a mask layer on the process subject, and form a silicon-containing layer. As a result, the plasma resistance of the mask layer is remarkably improved as compared to the mask layer itself.

Since the layer formed by the sputtering on the surface of the mask layer contains silicon as the main component, it is difficult to apply this method to a process subject that includes a silicon etching objective layer. This is so, because, where the mask layer surface and etching objective layer consist of the same material, their etching rates become almost the same. On the other hand, this method may be applied to another etching objective layer, such as SiO_2, SiC, SiN, organic low dielectric constant body, SiOF, metal, or metal compound.

A second invention is directed to the point that a CVD method is used to form a silicon-containing layer on the surface of a mask layer that covers an etching objective layer and has an opening formed therein. As a raw material gas for the silicon-containing layer, either an organic silane group gas or inorganic silane group gas can be used. However the inorganic silane group gas is preferably used.

In a third invention, a silicon compound, such as SiF_4, is added to an etching gas to improve the plasma resistance of an ArF photoresist mask layer, while etching an etching objective layer at the same time.

In these inventions, a process of removing the mask layer (ashing) follows the etching of the etching objective layer. At this time, the silicon-containing layer is present on the surface of the mask layer. Where a plurality of stages are performed to remove the silicon-containing layer and the mask layer itself separately from each other, the removal operations can be respectively performed in accordance with the natures of these layers. As a matter of course, the mask layer may be removed at once. It is determined which to use, based on comparison in the total advantages and disadvantages between the removal using a plurality of stages and the removal performed at once.

Where a plurality of stages is used to remove the mask layer, the first step uses plasma of a gas

containing a fluorine compound, to remove or plasma-etch the silicon-containing layer, and the second step removes the mask layer itself. Where the mask layer is made of a resist material, such as an ArF photoresist, the second step uses plasma of a gas containing no fluorine compound, such as O_2, N_2 and H_2, to remove the mask layer. Where the mask layer is an ArF photoresist layer, the gas containing a fluorine compound used in the first step is preferably CF_4. This is so, because the ArF photoresist layer below the silicon-containing layer is less damaged by CF_4.

Furthermore, where the etching objective layer consists of silicon oxide, the etching gas contains at least one selected from the group consisting of C_4F_6, C_4F_8, and C_5F_8.

[Embodiments of the Invention]

FIG. 1 is a sectional view showing a processing apparatus 1, which can perform the present invention. There is a process container 2, which is made of a metal, such as aluminum with an anodized surface, and is grounded for safety. The process container 2 is provided with a susceptor (first electrode) 5 disposed therein on the bottom through an insulator 3 and functioning as the lower electrode of parallel-plate electrodes. A high-pass filter (HPF) 6 is connected to the susceptor 5. An electrostatic chuck 11 is provided

on the susceptor 5 to place a process subject W, such as a semiconductor wafer, thereon. The process subject W has an etching objective layer of a silicon oxide layer or the like, and a mask layer of an ArF photoresist layer or the like, covering the etching objective layer, and having an opening formed therein. The ArF photoresist may be made of an alicyclic group-containing acrylate resin, cycloolefin resin, cycloolefin-maleic anhydride resin, or the like. The etching objective layer is not limited to the silicon oxide layer. The etching objective layer may consist of oxide film (oxygen compound) such as TEOS, BPSG, PSG, SOG, thermal oxidation film, HTO, FSG, organic silicon oxide film, CORAL (Novellus Systems), low dielectric constant organic insulating film, or the like.

The electrostatic chuck 11 is arranged such that an electrode 12 is sandwiched between insulators. The electrode 12 is supplied with a DC voltage from a DC power supply 13 connected thereto, so that the process subject W is attracted and held by means of electrostatic force. A focus ring 15 made of silicon or the like is disposed around the process subject W to improve etching uniformity.

An upper electrode (second electrode) 21 is disposed above the susceptor 5 to face the susceptor 5. The upper electrode 21 is supported by an upper portion of the process container 2 through an insulator 22.

The upper electrode 21 is formed of an electrode plate 24, which is made of silicon or the like and has a structure as a showerhead, and a support body 25 that supports the electrode plate 24.

A gas inlet port 26 is formed at the center of the support body 25. The gas inlet port 26 is connected to a gas supply line 27, valve 28, mass-flow controller 29, and process gas supply source 30 in this order. The process gas supply source 30 can supply Ar, Kr, Xe and the like, CF_4, C_4F_6, C_4F_8, C_5F_8, and the like, and O_2, N_2, H_2, and the like.

On the other hand, the bottom of the process container 2 is connected to an exhaust line 31, which is connected to an exhaust device 35. The process container 2 is provided with a gate valve 32 on the sidewall, so that the process subject W can be transferred between the process container 2 and an adjacent load-lock chamber (not shown).

The upper electrode 21 is connected to a low-pass filter (LPF) 42, and also to a first high-frequency power supply 40 through a matching device 41. The susceptor 5 functioning as the lower electrode is connected to a second high-frequency power supply 50 through a matching device 51. The structure of the processing apparatus is not limited to that shown in FIG. 1.

Next, an explanation will be give of the procedure

for processing the process subject W.

The gate valve 32 is first opened, and the process subject W is transferred into the process container 2 and placed on the electrostatic chuck 11. Then, the gate valve 32 is closed, and the pressure in the process container 2 is reduced by the exhaust device 35. Then, the valve 28 is opened, and an inert gas, such as Ar, is supplied from the process gas supply source 30, thereby setting the pressure in the process container 2 at, e.g., 1.33 Pa (10 mTorr). In this state, high-frequency powers are applied to the upper electrode 21 and the lower electrode, or susceptor 5 to ionize at least part of the Ar, thereby sputtering the focus ring 15. Before or after the timing when the high-frequency powers are applied to the upper and lower electrodes, a DC voltage is applied from DC power supply 13 to the electrode 12 in the electrostatic chuck 11 to electrostatically attract and hold the process subject W on the electrostatic chuck 11. The high-frequency power applied to the upper electrode 21 provides energy for urging ionization of the inert gas. This power is set to have a frequency of 60 MHz and a power of 2,000W. The high-frequency power applied to the susceptor 5 is set to have a frequency of 2 MHz and a power of 100W. In this step, a silicon-containing layer is formed on the surface of the mask layer. If the time used to form silicon-containing layer on the surface of the

mask layer is too short, the plasma resistance improvement effect can be hardly obtained. If the time is too long, a lot of silicon-containing layer is formed on the surface of the etching objective layer in an opening portion of the mask layer, and hinders the etching performed thereafter. In this embodiment, it was confirmed that a range of 60 to 90 seconds was preferable. As regards the powers, this embodiment reduced variation in the opening shape of the mask layer when the silicon-containing layer was formed, as compared to a case where the power applied to the upper electrode was set at 1,250W, and the power applied to the susceptor was set at 400W (a so-called low VPP). If the VPP is too high, the opening of the mask layer is expanded, thereby making it difficult to form holes or grooves in accordance with the designed opening pattern in the following etching step. After the formation of the silicon-containing layer on the surface of the mask layer is finished, the high-frequency powers stop being supplied.

Then, an etching gas is supplied into the process container 2. For example, where the etching objective layer is a silicon oxide layer, the etching gas is a mixture gas of C_4F_6, O_2, and Ar. The pressure in the process container 2 is set at, e.g., 2.67 Pa (20 mTorr), and the high-frequency powers applied to the upper electrode 21 and susceptor 5 are set at, e.g., 1,600W

and 800W, respectively. The frequencies of the high-frequency powers at this time are set at the same values as in the sputtering. The high-frequency powers are applied to turn the etching gas into plasma, thereby etching the etching objective layer, or silicon oxide layer. After the etching is finished, the etching gas and high-frequency powers stop being supplied. In this etching step, the selectivity of the silicon oxide layer relative to the mask layer (the etching rate of the silicon oxide layer / the etching rate of the mask layer) was 28.8. Where the etching was performed without the silicon-containing layer formed on the surface of the mask layer, the selectivity was 8.2.

The etching performed as described above is followed by a step of removing the mask layer (ashing step). In this example, a plurality of stages are used to remove the mask layer.

In the first stage, for example, CF_4 is supplied into the process container 2, thereby setting the pressure in the process container 2 at, e.g., 6.66 Pa (50 mTorr). The high-frequency powers applied to the upper electrode 21 and susceptor 5 are set at, e.g., 1,600W and 800W, respectively. These powers have frequencies the same as those in the sputtering or etching. This process is performed for a predetermined time of, e.g., 90 seconds, removing almost all the

silicon-containing layer formed on the mask layer by plasma of CF_4. This is done, because, if the silicon-containing layer is left, silicon-containing products may stick to the surface of the process subject after the mask layer is removed in the next second stage. When a gas containing CF_4, and O_2 and Ar added thereto was used at this stage, the mask layer of an ArF photoresist was damaged. Accordingly, it is preferable to use a gas containing only CF_4, or a gas containing CF_4 with a small amount of O_2 and Ar added thereto.

In the second stage, the pressure, high-frequency powers, high-frequency power supply frequencies were not changed from the first stage, but only the process gas was changed. O_2 was used as the process gas. Other than O_2, a mixture gas of N_2 and H_2, or the like may be used. The process subject was observed after the mask layer was removed. As a result, the opening shape and sectional shape of holes and grooves almost accorded with the design. Furthermore, there was no silicon-containing product sticking to the process subject.

[Claims]

1. A method of processing a process subject, comprising the steps of:

placing a process subject on a susceptor disposed in a process container, wherein the process subject has an etching objective layer, and a mask layer covering the etching objective layer and having an opening formed therein;

supplying an inert gas into the process container in a state where the process subject and a member having a surface at least a part of which is made of silicon are present in the process container;

supplying the process container with energy to ionize at least a part of the inert gas;

supplying an etching gas into the process container, and turning the etching gas into plasma; and

plasma-etching the etching objective layer through the opening of the mask layer in the process container.

2. The method of processing a process subject according to claim 1, further comprising a step of plasma-removing the mask layer by a plurality of stages, after the plasma etching step.

3. The method of processing a process subject according to claim 2, wherein the step of plasma-removing the mask layer by a plurality of stages comprises a first removing step of removing a part of the mask layer by plasma of a gas containing a fluorine

compound, and a second removing step of removing at least a part of the mask layer left by the first removing step, by plasma of a gas containing no fluorine compound.

4. The method of processing a process subject according to claim 3, wherein the mask layer is an ArF photoresist layer, and the gas used in the first removing step is CF_4.

5. The method of processing a process subject according to any one of claims 1 to 4, wherein the etching objective layer consists of silicon oxide, and the etching gas contains at least one selected from the group consisting of C_4F_6, C_4F_8, and C_5F_8.

6. The method of processing a process subject according to any one of claims 1 to 5, wherein the member having a surface at least a part of which is made of silicon is a focus ring disposed around the process subject.

7. The method of processing a process subject according to any one of claims 1 to 5, wherein the member having a surface at least a part of which is made of silicon is a showerhead disposed to supply the etching gas into the process container.

8. The method of processing a process subject according to any one of claims 1 to 5, wherein the member having a surface at least a part of which is made of silicon is a semiconductor wafer.

9. The method of processing a process subject according to any one of claims 1 to 3 and 6 to 8, wherein the mask layer is an ArF photoresist layer.

10. The method of processing a process subject according to claim 1, further comprising a step of supplying the susceptor with a high-frequency power.

11. The method of processing a process subject according to any one of claims 1 to 10, wherein the energy is high-frequency energy.

12. The method of processing a process subject according to any one of claims 1 to 10, wherein the step of supplying the process container with energy comprises a step of applying a high-frequency power to an antenna disposed outside the process container.

13. The method of processing a process subject according to any one of claims 1 to 10, wherein the step of supplying the process container with energy comprises a step of applying a high-frequency power to a counter electrode disposed in the process container to face the susceptor.

14. A method of processing a process subject, comprising the steps of:

placing a process subject on a susceptor disposed in a process container, wherein the process subject has an etching objective layer, and a mask layer covering the etching objective layer and having an opening formed therein;

forming a silicon-containing layer on a surface of the mask layer in the process container;

supplying an etching gas into the process container, and turning the etching gas into plasma; and

plasma-etching the etching objective layer through the opening of the mask layer in the process container.

15. The method of processing a process subject according to claim 14, wherein the step of forming a silicon-containing layer comprises a step of using a PVD method.

16. The method of processing a process subject according to claim 14, wherein the step of forming a silicon-containing layer comprises a step of using a CVD method.

17. The method of processing a process subject according to any one of claims 14 to 16, further comprising a step of plasma-removing the mask layer by a plurality of stages, after the plasma etching step.

18. The method of processing a process subject according to claim 17, wherein the step of plasma-removing the mask layer by a plurality of stages comprises a first removing step of removing a part of the mask layer by plasma of a gas containing a fluorine compound, and a second removing step of removing at least a part of the mask layer left by the first removing step, by plasma of a gas containing no fluorine compound.

19. The method of processing a process subject according to claim 18, wherein the mask layer is an ArF photoresist layer, and the gas used in the first removing step is CF_4.

20. The method of processing a process subject according to any one of claims 14 to 19, wherein the etching objective layer consists of silicon oxide, and the etching gas contains at least one selected from the group consisting of C_4F_6, C_4F_8, and C_5F_8.

21. The method of processing a process subject according to any one of claims 14 to 18 and 20, wherein the mask layer is an ArF photoresist layer.

22. A method of processing a process subject, comprising the steps of:

placing a process subject on a first electrode disposed in a process container, wherein the process container has a member having a surface at least a part of which is made of silicon, the first electrode, and a second electrode facing the first electrode, and the process subject has an etching objective layer, and a mask layer covering the etching objective layer and having an opening formed therein;

supplying an inert gas into the process container;

applying a high-frequency power to the first electrode;

applying a high-frequency power to the second electrode;

supplying an etching gas into the process container, and turning the etching gas into plasma; and

plasma-etching the etching objective layer through the opening of the mask layer in the process container.

23. The method of processing a process subject according to claim 22, wherein the member having a surface at least a part of which is made of silicon is an electrode plate of the second electrode.

24. The method of processing a process subject according to claim 22, further comprising a step of plasma-removing the mask layer by a plurality of stages, after the plasma etching step.

25. A method of processing a process subject, comprising the steps of:

placing a process subject on a susceptor disposed in a process container, wherein the process subject has an etching objective layer, and an ArF photoresist mask layer covering the etching objective layer and having an opening formed therein;

supplying an etching gas containing a silicon compound into the process container, and turning the etching gas into plasma; and

plasma-etching the etching objective layer through the opening of the ArF photoresist mask layer in the process container.

26. The method of processing a process subject according to claim 25, wherein the silicon compound is

SiF_4.

(Drawing)

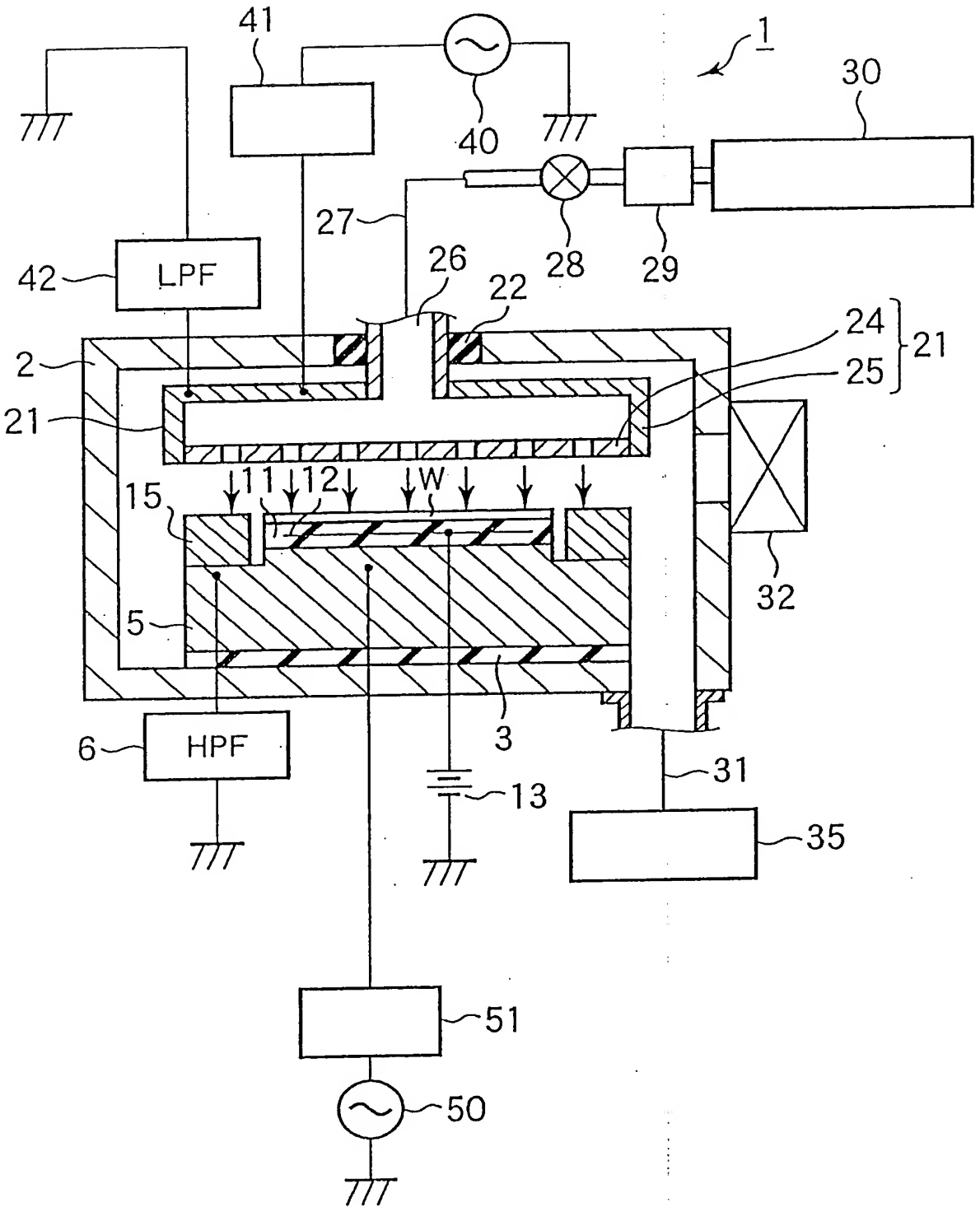

Fig. 1